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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,166	04/20/2001	Katsumi Ichinose	1095.1184	9022
21171	7590	06/20/2005	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			VO, LILIAN	
		ART UNIT	PAPER NUMBER	
		2195		

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/838,166	ICHINOSE ET AL.	
	Examiner Lilian Vo	Art Unit 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 24 March 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1 - 4 and 7 - 8 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1 - 4 and 7 - 8 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

1. Claims 1 – 4 and 7 – 8 are pending. Claims 5 – 6 have been canceled.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/20/05 has been entered.

***Claim Rejections - 35 USC § 101***

3. 35.U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.
4. Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.
5. **Claims 1, 2 and 7** are directed to method steps, which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. Moreover, each of the claimed steps, inter alia, dividing, instructing, comparing, determining, can be practiced mentally in conjunctions with pen and paper. The claimed steps do not define a machine or computer implemented process [see MPEP 2106]. Therefore, the claimed invention

is directed to non-statutory subject matter. (The examiner suggests applicant to change “method” to “computer implemented method” in the preamble to overcome the outstanding 35 U.S.C. 101 rejection).

6. Regarding **claims 8**, the system is at best a software system, per se, failing to be tangibly embodied or include any recited hardware as part of the system.

*Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kametani in view of Lewis (US 6,378,066).

9. Regarding **claim 1**, Kametani discloses an information processing method for causing a computing device having a plurality of processors to carry out predetermined information processing, the information processing method comprising:

dividing a program to be executed into a plurality of parallel processing blocks (abstract, col. 12, lines 52 - 63);

dividing said parallel processing blocks into threads which are basic units to be assigned respectively to said plurality of processors for being processed thereby (abstract, col. 12, lines 52 - 63); and

instructing a predetermined processor to execute a next parallel processing block when said predetermined processor has terminated execution of a respective thread assigned thereto (abstract, col. 2, lines 55 – 61, col. 4, line 66 – col. 5, line 19, col. 13, lines 22 – 26, col. 14, lines 36 – 49).

Kametani however did not clearly the additional limitation as claimed. Nevertheless, Lewis discloses the instruction step comprises:

comparing a first parallel block number processing control information region corresponding to a parallel processing block executed by a foremost thread and a second parallel block number of a thread information region which corresponds to the respective thread assigned to the predetermined processor (abstract, col. 9, line 60 – col. 10, line 40), and

determining whether a corresponding thread of the predetermined processor should execute said next parallel processing block based upon the comparison results, wherein

when execution is required, determining said next parallel processing block to be executed by the predetermined processor with reference to said second parallel block number, and generating a parallel processing block control information region corresponding to said next parallel processing block, wherein a number of threads executed in said next parallel processing block are stored, and said corresponding thread of the predetermined processor executing said next parallel processing block, and

when execution is not required, determining a parallel processing block to be executed with reference to said second parallel processing block number and executing said parallel processing block (col. 3, line 47 – col. 4, line 7, col. 5, line 50 – col. 6, line 46, col. 9, line 60 – col. 10, line 43).

It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate Lewis's teaching together with Kametani to make effective use of processor resource in parallel processing and still able to maintain the dependency relationship between blocks as appropriately (col. 3, lines 50 – 55).

10. Regarding **claim 2**, Kametani discloses that when a predetermined instruction is given in the program to be executed, execution of a next parallel processing block is not instructed until processing of all of the threads have been terminated (abstract, col. 13, lines 27 – 31 and col. 14, lines 50 - 67).

11. **Claims 3 – 4** are rejected on the same ground as stated in claim 1 above.

*Claim Rejections - 35 USC § 102*

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 7 – 8 are rejected under 35 U.S.C. 102(e) as being anticipate by Lewis (US 6,378,066).

14. Regarding **claim 7**, Lewis discloses a method comprising:

dividing a program to be executed into a plurality of parallel processing block (abstract, col. 3, line 47 – col. 4, line 7);

dividing the parallel processing blocks into threads to be respectively assigned to a plurality of processors (figs. 10A – 10C, col. 9, line 61 – col. 10, line 3);

designating a parallel processing block number to each of the assigned threads corresponding to the parallel processing block being executed by the assigned threads at a predetermined time (fig. 10a – 10c, and col. 10, lines 4 – 20);

comparing the parallel processing block number corresponding to a leading thread of the assigned threads to a parallel block number corresponding to each of the assigned threads (col. 10, lines 4 – 20 and figs. 10a – 10c); and

determining whether the leading thread should execute a next parallel processing block, wherein when execution is required, determining the next parallel processing block to be executed with reference to the parallel processing block number of the leading thread (col. 5, line 65 – col. 6, line 44, col. 10, lines 20 – 40, col. 12, lines 15 - 23).

15. **Claim 8** is rejected on the same ground as stated in claim 7 above.

*Response to Arguments*

16. Applicant's arguments filed 3/24/05 have been fully considered but they are not persuasive for the reason set forth below.

17. Regarding applicant's arguments that Lewis fails to disclose "comparing a first parallel block number processing control information region corresponding to a parallel processing block

executed by a foremost thread and a second parallel block number of a thread information region which corresponds to the respective thread assigned to the predetermined processor, and determining whether a corresponding thread of the predetermined processor should execute said next parallel processing block...” (page 6, 5<sup>th</sup> paragraph), the examiner disagrees. Lewis clearly discloses such teachings in abstract, col. 3, line 47 – col. 4, line 7, col. 5, line 50 – col. 6, line 46 and col. 9, line 60 – col. 10, line 43).

18. In response to applicant's argument (page 7, 2<sup>nd</sup> paragraph) that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a thread being able to proceed to a next block without having to wait for the remaining threads to execute a block already executed by the thread) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, with respect to applicant's remarks that Lewis discloses a thread being able to skip a block if the block is dependent upon other blocks (page 7, 2<sup>nd</sup> paragraph, last sentence), applicant is directed to col. 10, lines 35 – 40 to recognize when a thread skip the processing blocks, it does not stay idle by not using computing resources efficiently, but it continue to process other queued blocks depending upon the dependency relationships associated with each block in the queue.

19. Applicant's arguments with respect to claims 2, 7 and 8 (page 7, 5<sup>th</sup>, 7<sup>th</sup> and 8<sup>th</sup> paragraph) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims

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define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist at 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo  
Examiner  
Art Unit 2127

*M. Vo*  
MENGAL T. AN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER